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Electronic Design Automation for IC System Design, Verification, and Testing Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

SystemC: From the Ground Up, Second Edition David C. Black,Jack Donovan,Bill Bunton,Anna Keist,2009-12-18 SystemC provides a robust set of extensions to the C language that enables rapid development of complex models of hardware and software systems The authors focus on practical use of the language for modeling real systems showing A step by step build up of syntax Code examples for each concept Updates to reflect the SystemC standard IEEE 1666 Why features are as they are Many resource references How SystemC fits into an ESL methodology This new edition of an industry best seller is updated to reflect the standardization of SystemC as IEEE 1666 and other improvements that reflect feedback from readers of the first edition The wide ranging feedback also include suggestions from editors of the Japanese and Korean language translations professors and students and computer engineers from a broad industrial and geographical spectrum all who have successfully used the first edition New chapters have been added on the SystemC Verification Library and the Transaction Level Modeling and proposed changes to the current SystemC standard David Black and Jack Donovan well known consultants in the EDA industry have teamed with Bill Bunton and Anna Keist experienced SystemC modeling engineers to write the second edition of this highly popular classic As a team the authors bring over 100 years of ASIC and system design experience together to make a very readable introduction to SystemC   Models, Methods, and Tools for Complex Chip Design Jan Haase,2013-09-18 This book brings together a selection of the best papers from the fifteenth edition of the Forum on specification and Design Languages Conference FDL which was held in September 2012 at Vienna

University of Technology Vienna Austria FDL is a well established international forum devoted to dissemination of research results practical experiences and new ideas in the application of specification design and verification languages to the design modeling and verification of integrated circuits complex hardware software embedded systems and mixed technology systems **FPGA Design** Philip Andrew Simpson,2015-05-19 This book describes best practices for successful FPGA design It is the result of the author s meetings with hundreds of customers on the challenges facing each of their FPGA design teams By gaining an understanding into their design environments processes what works and what does not work key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed This book s content has a strong focus on design teams that are spread across sites The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams enabling the exchange of design blocks across teams Coverage includes the complete FPGA design flow from the basics to advanced techniques This new edition has been enhanced to include new sections on System modeling embedded design and high level design The original sections on Design Environment RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers Presents complete field tested methodology for FPGA design focused on reuse across design teams Offers best practices for FPGA timing closure in system debug and board design Details techniques to resolve common pitfalls in designing with FPGAs **ESL Design and Verification** Grant Martin,Brian Bailey,Andrew Piziali,2010-07-27 Visit the authors companion site http www electronicsystemlevel com Includes interactive forum with the authors Electronic System Level ESL design has mainstreamed it is now an established approach at most of the world s leading system on chip SoC design companies and is being used increasingly in system design From its genesis as an algorithm modeling methodology with no links to implementation ESL is evolving into a set of complementary methodologies that enable embedded system design verification and debug through to the hardware and software implementation of custom SoC system on FPGA system on board and entire multi board systems This book arises from experience the authors have gained from years of work as industry practitioners in the Electronic System Level design area they have seen SLD or ESL go through many stages and false starts and have observed that the shift in design methodologies to ESL is finally occurring This is partly because of ESL technologies themselves are stabilizing on a useful set of languages being standardized SystemC is the most notable and use models are being identified that are beginning to get real adoption ESL DESIGN VERIFICATION offers a true prescriptive guide to ESL that reviews its past and outlines the best practices of today Table of ContentsCHAPTER 1 WHAT IS ESL CHAPTER 2 TAXONOMY AND DEFINITIONS FOR THE ELECTRONIC SYSTEM LEVEL CHAPTER 3 EVOLUTION OF ESL DEVELOPMENT CHAPTER 4 WHAT ARE THE ENABLERS OF ESL CHAPTER 5 ESL FLOW CHAPTER 6 SPECIFICATIONS AND MODELING CHAPTER 7 PRE PARTITIONING ANALYSIS CHAPTER 8 PARTITIONING CHAPTER 9 POST

PARTITIONING ANALYSIS AND DEBUG CHAPTER 10 POST PARTITIONING VERIFICATION CHAPTER 11 HARDWARE IMPLEMENTATION CHAPTER 12 SOFTWARE IMPLEMENTATION CHAPTER 13 USE OF ESL FOR IMPLEMENTATION VERIFICATION CHAPTER 14 RESEARCH EMERGING AND FUTURE PROSPECTS APPENDIX LIST OF ACRONYMS Provides broad comprehensive coverage not available in any other such book Massive global appeal with an internationally recognised author team Crammed full of state of the art content from notable industry experts **Model-Implementation Fidelity in Cyber Physical System Design** Anca Molnos,Christian Fabre,2016-12-08 This book puts in focus various techniques for checking modeling fidelity of Cyber Physical Systems CPS with respect to the physical world they represent The authors present modeling and analysis techniques representing different communities from very different angles discuss their possible interactions and discuss the commonalities and differences between their practices Coverage includes model driven development resource driven development statistical analysis proofs of simulator implementation compiler construction power temperature modeling of digital devices high level performance analysis and code device certification Several industrial contexts are covered including modeling of computing and communication proof architectures models and statistical based validation techniques *System Design with SystemC™* Thorsten Grötker,2002-05-31 The emergence of the system on chip SoC era is creating many new challenges at all stages of the design process Engineers are reconsidering how designs are specified partitioned and verified With systems and software engineers programming in C C and their hardware counterparts working in hardware description languages such as VHDL and Verilog problems arise from the use of different design languages incompatible tools and fragmented tool flows Momentum is building behind the SystemC language and modeling platform as the best solution for representing functionality communication and software and hardware implementations at various levels of abstraction The reason is clear increasing design complexity demands very fast executable specifications to validate system concepts and only C C delivers adequate levels of abstraction hardware software integration and performance System design today also demands a single common language and modeling foundation in order to make interoperable system level design tools services and intellectual property a reality SystemC is entirely based on C C and the complete source code for the SystemC reference simulator can be freely downloaded from www systemc org and executed on both PCs and workstations System Design and SystemC provides a comprehensive introduction to the powerful modeling capabilities of the SystemC language and also provides a large and valuable set of system level modeling examples and techniques Written by experts from Cadence Design Systems Inc and Synopsys Inc who were deeply involved in the definition and implementation of the SystemC language and reference simulator this book will provide you with the key concepts you need to be successful with SystemC System Design with SystemC thoroughly covers the new system level modeling capabilities available in SystemC 2 0 as well as the hardware modeling capabilities available in earlier versions of SystemC designed and implemented the SystemC language and reference simulator this book will

provide you with the key concepts you need to be successful with SystemC System Design with SystemC will be of interest to designers in industry working on complex system designs as well as students and researchers within academia All of the examples and techniques described within this book can be used with freely available compilers and debuggers no commercial software is needed Instructions for obtaining the free source code for the examples obtained within this book are included in the first chapter *Combining Formal Model-based System-level Design with SystemC Transaction Level Modeling* Jens Gladigau,2012 **System Level Modeling and Design Using SysML and SystemC** Waseem Mohamed Raslan,American University in Cairo,2007 Transaction-Level Modeling with SystemC Frank Ghenassia,2005-11-28 Suitable for bookstore catalogue *Formal Methods and Models for System Design* Rajesh Gupta,Paul Le Guernic,Sandeep Kumar Shukla,Jean-Pierre Talpin,2004-06-30 Perhaps nothing characterizes the inherent heterogeneity in embedded sys tems than the ability to choose between hardware and software implementations of a given system function Indeed most embedded systems at their core repre sent a careful division and design of hardware and software parts of the system To do this task effectively models and methods are necessary functionality to capture application behavior needs and system implementation constraints Formal modeling can be valuable in addressing these tasks As with most engineering domains co design practice defines the state of the it seeks to add new capabilities in system conceptualization mod art though eling optimization and implementation These advances particularly those related to synthesis and verification tasks direct1y depend upon formal under standing of system behavior and performance measures Current practice in system modeling relies upon exploiting high level programming frameworks such as SystemC EstereI to capture design at increasingly higher levels of ab straction and attempts to reduce the system implementation task While raising the abstraction levels for design and verification tasks to be really useful these approaches must also provide for reuse adaptation of the existing intellectual property IP blocks Automatic Generation of Transaction Level Models Lucky Lochi Yu Lo,2010-08-01 The rising complexity in system designs over the past decades poses great challenges to current designers One way to cope with this challenge has been to raise the level of abstraction of design reducing the number of elements and speeding up design decisions Transaction Level Models TLM have emerged as a new alternative to design Multi Processor System on Chips MPSoC This book aims to contribute in different aspects a definition of a modeling style for SystemC TLMs a definition of a data structure complete and flexible enough to describe a complete embedded system and generation algorithms that would use it to automatically produce an executable TLM in SystemC With this approach automatic generation of TLMs can be achieved freeing the designer from error prone manual coding and allowing a focus on higher level design decisions speeding up the overall design phase **System Level Design with .Net Technology** El Mostapha Aboulhamid,Frederic Rousseau,2018-10-03 The first book to harness the power of NET for system design System Level Design with NET Technology constitutes a software based approach to design modeling verification and simulation World class developers

who have been at the forefront of system design for decades explain how to tap into the power of this dynamic programming environment for more effective and efficient management of metadata and introspection and interoperability between tools Using readily available technology the text details how to capture constraints and requirements at high levels and describes how to percolate them during the refinement process Departing from proprietary environments built around System Verilog and VHDL this cutting edge reference includes an open source environment ESys NET that readers can use to experiment with new ideas algorithms and design methods and to expand the capabilities of their current tools It also covers Modeling and simulation including requirements specification IP reuse and applications of design patterns to hardware software systems Simulation and validation including transaction based models accurate simulation at cycle and transaction levels cosimulation and acceleration technique as well as timing specification and validation Practical use of the ESys NET environment Worked examples end of chapter references and the ESys NET implementation test bed make this the ideal resource for system engineers and students looking to maximize their embedded system designs **System Level Design with SystemC** Daghan S. Altas,2000 In this thesis we provide a system level design methodology aimed for the design of embedded systems Our methodology is geared towards the concurrent design of hardware components and software agents Our choice of tool language pair is CoWare N2C design tool and SystemC specification language Our design flow is completed with a high performance hardware synthesis methodology relying behavioral synthesis A case study the design of an ATM switch is carried out to illustrate the proposed ideas *The Engineering Design of Systems* Dennis M. Buede,William D. Miller,2024-04-16 The Engineering Design of Systems Comprehensive resource covering methods to design verify and validate systems with a model based approach addressing engineering of current software centric systems The newly revised and updated Fourth Edition of The Engineering Design of Systems includes content addressing model based systems engineering digital engineering digital threads AI SysML 1 0 and 2 0 digital twins and GENESYS software The authors explore system and software centric architecture allocations and logical and physical architecture development including revised terminologies for a variety of subsections throughout Composed of 15 chapters this book includes important new sections on modeling approaches for middle out engineering reverse engineering and agile systems engineering with a separate section on emerging trends within systems engineering to explore the most update to date methods The authors include comprehensive diagrams and a separate chapter on a complete exercise of the System Engineering process ranging from the operational concept to integration and qualification To aid in reader comprehension and retention of concepts the text is embedded with problems at the end of each chapter along with relevant case studies Sample topics covered in The Engineering Design of Systems include Structural system models to executable models verification and validation on systems of systems and external systems and context modeling Digital engineering digital threads artificial augmented intelligence AI stakeholder requirements and scientific foundations for systems engineering

Quantifying a context and external systems model including intended and unintended inputs both deterministic and non deterministic Functional architecture development logical and physical architecture development allocated architecture development interface design and decision analysis for design trades The Engineering Design of Systems is highly suitable as a main text for undergraduate and graduate students studying courses in system engineering design systems architecture and systems integration The text is also valuable as a reference for practicing system architects systems engineers industrial engineers engineering management professionals and systems integrators **TLM 2.0: From the Ground Up** David Black,Hermendra Talesara,2012-07-31 Following the popular second edition of SystemC From the Ground Up this book continues in providing accessible information on how to create and use TLM 2 0 models in SystemC Concepts are carefully described followed by syntax and application examples Exercises at the end of each chapter will give the reader practice material System-level Design Refinement Using SystemC Robert Dale Walstrom,2005 Embedded systems have become increasingly complex with the advent of the system on a chip SOC era Today a typical SOC may consist of one or more processor cores dedicated hardware processing units peripheral devices on chip memories and the logic for a sophisticated communications network to link all of these components together In order to deal with the complexity of designing a SOC designers needed new design languages and tools System level design languages SLDLs and EDA tools allow designers to manage this complexity by using different levels of abstraction to define and model the system Several SLDLs have been introduced in recent years most notably SpecC developed at the University of California Irvine and SystemC developed by the Open SystemC Initiative OSCI In some aspects these SLDLs share the same goals Both support the ability to model a system at various levels of abstraction and the reuse of intellectual property However while SystemC claims the most industry support with a wide variety of supported tools available from major EDA vendors it lacks a well defined refinement methodology like that of SpecC The SpecC refinement methodology leads designers from its highest level of abstraction down to its lowest level of abstraction While each level of abstraction in SystemC is clearly defined it is not clear what changes need to be made to convert a design from one level of abstraction to another In order to facilitate a system level design approach SystemC needs well defined methodology for bringing a model defined at the highest level of abstraction down to the lowest level of abstraction This thesis presents a top down refinement methodology for systems modeled in SystemC Since SystemC has gained widespread industry support such a methodology would make it easier for designers who use SystemC to refine their design and use the SystemC language as intended by a system level design approach **SystemC Kernel Extensions for Heterogeneous System Modeling** Hiren Patel,Sandeep Kumar Shukla,2008-11-01 SystemC Kernel Extensions for Heterogeneous System Modeling is a result of an almost two year endeavour on our part to understand how SystemC can be made useful for system level modeling at higher levels of abstraction Making it a truly heterogeneous modeling language and platform for hardware software co design as well as complex embedded hardware

designs has been our focus in the work reported in this book   *System-level Design* Moshe Meyassed,1997   <u>System-level Modeling and Design with the SpecC Language</u> Rainer Dömer,2000

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